

**AMENDMENT AND RESPONSE**

Serial No.: 09/992,880

Filing Date: November 5, 2001

Title: INTEGRATED CIRCUIT WITH A MOS CAPACITOR

**PAGE 11**

Attorney Docket No. 125.014US01

**REMARKS**

Claims 1-5, 8-37, 56-64 are pending in this application. Claims 6 and 7 have been withdrawn from consideration. Claims 38-55 have been canceled. Claims 56-64 have been added. Claims 1-5, 8-17, 20 and 23-29 are rejected. Claims 18, 19, 21, 22 and 30-32 are objected to.

**Rejection Under 35 U.S.C. §112**

Claim 13 was rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Applicant has amended Claim 13. As amended Claim 13 clearly contains subject matter described in the specification in such a way to enable one skilled in the art to make and/or use the invention. An example of this includes contact opening 107 and base 112 of Figure 4A as well as paragraph 36 and Figure 4E and paragraph 38 of the present application. Therefore, Applicant respectfully requests the withdrawal of the 35 U.S.C. §112, first paragraph rejection of Claim 13.

**Rejection Under 35 U.S.C. §102(b)**

Claims 1-5, 8-17, 20, 23, 24 and 29 were rejected under 35 U.S.C. §102(b) as being anticipated by Chang et al. (U.S. Patent 5,792,681).

**Claims 1-5 and 8-9**

In regards to independent Claim 1, Applicant has reviewed the rejection and the Chang et al. reference and respectfully traverses the rejection of Claim 1 under U.S.C. §102(b). Claim 1 includes the method of "patterning the layer mask to expose a pre-selected portion of the dielectric layer" (emphasis added). One embodiment of this aspect of the present invention is illustrated Figure 6B and discussed in paragraph 44 of the current application. The Chang et al. reference does not teach "patterning the layer mask to expose a pre-selected portion of the dielectric layer," as is disclosed and claimed in Claim 1 of the present application. Please

**AMENDMENT AND RESPONSE****PAGE 12**

Serial No.: 09/992,880

Attorney Docket No. 125.014US01

Filing Date: November 5, 2001

Title: INTEGRATED CIRCUIT WITH A MOS CAPACITOR

review, the BPSG layer 17 of Figure 9 and column 5, lines 17 of the Chang reference. Since a 102 (b) rejection requires a single art reference teach every aspect of the claimed invention and the Chang et al. reference does not, Claim 1 of the present invention is patentably distinct from the Chang et al. reference. Accordingly, Applicant respectfully request the withdrawal of the rejection of Claim 1 under U.S.C. §102(b).

In addition, since Claims 2-4 and 8-9 depend from and further define patentably distinct Claim 1, the withdrawal of the rejection of Claims 2-4 and 8-9 under U.S.C. §102(b) is further requested.

**Claims 10-14**

In regards to Claim 10, Applicant has reviewed the rejection and the Chang reference and respectfully traverses the rejection of Claim 10 under U.S.C. §102(b). Claim 10 includes a method of "forming an oxide layer on a *surface* of a substrate" (emphasis added). One embodiment illustrating this aspect of the present invention is shown in Figure 4A and described in paragraph 36 of the present application. The Chang et al. reference does not teach the "forming an oxide layer on a surface of the substrate," as is disclosed and claimed in Claim 10 of the present application. Please refer to polysilicon layer 8 and silicon oxide layer 9 of Figure 2 and the discussion in Column 3, lines 56-65 of the Chang et al. reference. Since a 102 (b) rejection requires that a single art reference teach every aspect of the claimed invention and the Chang et al. reference does not, Claim 10 of the present invention is patentably distinct from the Chang et al. reference. Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 1 under 35 U.S.C. §102(b).

In addition, since Claims 11-14 depend from and further define patentably distinct Claim 10, the withdrawal of the rejection of Claims 11-14 under 35 U.S.C. §102(b) is further requested.

Moreover in regards to Claim 12, the Chang et al. reference does not teach "using the dielectric layer in at least one of the isolation islands as a capacitor dielectric in forming a capacitor," (emphasis added) as is disclosed and claimed in Claim 15 of the present application. Embodiments of this aspect of the present invention are illustrated in Figures 3 and 4f and

**AMENDMENT AND RESPONSE****PAGE 13**

Serial No.: 09/992,880

Attorney Docket No. 125.014US01

Filing Date: November 5, 2001

Title: INTEGRATED CIRCUIT WITH A MOS CAPACITOR

discussed in paragraph 33 of the present invention. As illustrated in these embodiments, the capacitor dielectric layer 140 is positioned between the top plate 110 and the bottom plate 108 in the present application. Referring to the Chang et al reference and in particular Figure 10 and Column 5 lines 12-4 of the description, layers 14 and 11 are positioned between a bottom electrode 8 and an upper electrode 20b of capacitor 5. Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 12 under 35 U.S.C. §102(b).

**Claims 15-22**

In regards to independent Claim 15, Applicant respectfully traverses the 35 U.S.C. §102(b) rejection of Claim 15. First of all, as argued above in regards to Claim 10, a method of "forming an oxide layer on a *surface* of a substrate" (emphasis added) as is Claimed in Claim 15 of the present application is not taught by the Chang et al. reference. Accordingly, Claim 15 of the present invention is patentably distinct from the Chang et al. reference. In addition, Claim 15 includes the method of "using the dielectric layer in at least one of the isolation islands as a capacitor dielectric in forming a capacitor." As discussed above with reference to Claim 12, an embodiment illustrating the formation of a capacitor of the present invention is shown in Figures 4E and 4F of the present application. The Change et al. reference does not teach "using the dielectric layer in at least *one of the isolation islands* as a capacitor dielectric in forming a capacitor," (emphasis added) as is disclosed and claimed in Claim 15 of the present application. Please refer to column 3, lines 25-28 of the Chang et al. reference which states: "A field oxide region, (FOX) is thermally grown and used to *isolate* subsequent NFET regions, 3, form PFET regions, 4, and *also used as the underlying layer for a subsequent capacitor structure region, 5*"(emphasis added). Moreover, the Change et al. reference does not teach "using the *dielectric layer* in at least one of the isolation islands as a *capacitor dielectric* in forming a capacitor," (emphasis added) as is disclosed and claimed in Claim 15 of the present application and as is argued above in regards to the rejection of Claim 12 above. Please refer to Figure 10 and the description in Column 5 lines 12-41 of the Chang et al. application where layers 14 and 11 that are positioned between a bottom electrode 8 and an upper electrode 20b of capacitor 5.

**AMENDMENT AND RESPONSE**

Serial No.: 09/992,880

Filing Date: November 5, 2001

Title: INTEGRATED CIRCUIT WITH A MOS CAPACITOR

**PAGE 14**

Attorney Docket No. 125.014US01

Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 15 under 35 U.S.C. §102(b).

In addition, since Claims 16-21 depend from and further define patentably distinct Claim 15, the withdrawal of the rejection of Claims 16-21 under 35 U.S.C. §102(b) is further requested.

**Claim 23**

In regards to independent Claim 23, Applicant respectfully traverses the 35 U.S.C. §102(b) rejection of Claim 23. First of all, as argued above in regards to Claim 10 and Claim 15 a method of "forming an oxide layer on a *surface* of a substrate" (emphasis added) as is Claimed in Claim 23 of the present application is not taught by the Chang et al. reference. Accordingly, Claim 23 of the present invention is patentably distinct from the Chang et al. reference. In addition, Claim 23 includes the method of "using the dielectric layer in at least one of the isolation islands as a capacitor dielectric in forming a capacitor." One embodiment illustrating the formation of the capacitor of the present invention is shown in Figures 4E and 4F of the present application. The Chang et al. reference does not teach "using the dielectric layer in at least *one of the isolation islands* as a capacitor dielectric in forming a capacitor," (emphasis added) as is disclosed and claimed in Claim 23 of the present application. Please refer to column 3, lines 25-28 of the Chang et al. reference which states: "A field oxide region, (FOX) is thermally grown and used to *isolate* subsequent NFET regions, 3, form PFET regions, 4, and *also used as the underlying layer for a subsequent capacitor structure region, 5*"(emphasis added). Moreover, the Chang et al. reference does not teach "using the dielectric layer in at least one of the isolation islands as a *capacitor dielectric* in forming a capacitor," (emphasis added) as is disclosed and claimed in Claim 23 of the present application and as is argued in relation to the response to the rejection of Claim 12 above. Please refer to Figure 10 and the description in Column 5 lines 12-41 of the Chang et al. application where layers 14 and 11 that are positioned between a bottom electrode 8 and an upper electrode 20b of capacitor 5. Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 23 under 35 U.S.C. §102(b).

In addition, since Claims 24-32 depend from and further define patentably distinct Claim 23, the withdrawal of the rejection of Claims 24-32 under 35 U.S.C. §102(b) is further requested.

**AMENDMENT AND RESPONSE****PAGE 15**

Serial No.: 09/992,880

Attorney Docket No. 125.014US01

Filing Date: November 5, 2001

Title: INTEGRATED CIRCUIT WITH A MOS CAPACITOR

Rejection Under 35 U.S.C. §103(a)

Claims 25 and 27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Chang et al. previously applied, in view of Schroeder (U.S. Patent 4,296,429), newly cited.

In light of the arguments put forth above regarding independent Claim 23 and the following arguments, Applicant respectfully traverses the Examiner's rejections of claims 25 and 27 under 35 U.S.C. §103(a). Applicant respectfully asserts that neither the Chang et al. nor the Schroeder reference alone or in combination teach or suggest all the aspects of claims 25 and 27 and the claims they respectfully depend from. Accordingly, Applicant respectfully requests the withdrawal of the rejection of claims 25 and 27 under 35 U.S.C. §103(a).

Claim 26

Claim 26 was rejected under 35 U.S.C. §103(a) as being unpatentable over Chang et al. and Schroeder as applied to claim 25 above, and further in view of Choi (U.S. Patent 5,780,330).

In light of the arguments put forth above regarding independent Claim 23 and the following arguments: Applicant respectfully traverses the Examiner's rejection of Claim 26 under 35 U.S.C. §103(a). Applicant respectfully asserts that neither the Chang et al. nor the Schroeder reference alone or in combination teach or suggest all the aspects of claim 26 and the claim it depends from. Accordingly, Applicant respectfully requests the withdrawal of the rejection of claim 26 under 35 U.S.C. §103(a).

Allowable Subject Matter

Claims 18, 19, 21, 22 and 30-32 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Added claims

FEB-27-2003(THU) 17:22

FOGG AND ASSOCIATES, LLC

(FAX)612 677 3553

P. 018/018

**AMENDMENT AND RESPONSE**

Serial No.: 09/992,880

Filing Date: November 5, 2001

Title: INTEGRATED CIRCUIT WITH A MOS CAPACITOR

**PAGE 16**

Attorney Docket No. 125.014US01

Applicant has added claims 56-64 which are supported in the application as filed and are patentably distinct over the cited art of record.

**CONCLUSION**

Applicant respectfully submits that claims 1-5, 8-37 and 56-64 are in condition for allowance and notification to that effect is earnestly requested. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 332-4720.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 502432.

Respectfully submitted,



\_\_\_\_\_  
Scott V. Lundberg  
Reg. No. 41,958

Attorneys for Applicant  
Fogg & Associates, LLC  
P.O. Box 581339  
Minneapolis, MN 55458-1339  
T - (612) 332-4720  
F - (612) 677-3553

**FAX RECEIVED**

FEB 27 2003

TECHNOLOGY CENTER 2800